IBM PC Institute

Personal Systems Reference PC Processors

February 2004 - Version 272

Intel® Celeron® for value desktop systems

Code name	**Willamette**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD SSE2	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions) / Streaming SIMD Extensions 2 (144 new instructions)
L1 cache - bus	256-bit data path / full speed
L1 data cache	8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**128KB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
Frontside bus	**400MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz
Frontside bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software
Cache line size	128 bytes (32 bytes x 4 chunks); burst mode bus of addr-data-data-data
Multiple processors	No SMP support
Technology (micron)	0.18u
Transistors	~42 million with die size of 217 square millimeters
Package and connector	**Flip-Chip Pin Grid Array-2 (FC-PGA2) requires 478-pin surface mount Zero Insertion Force (ZIF) socket named mPGA478B socket; used with SDRAM-based chipset (such as 845 chipset)**
Frequency (MHz) and available date	1.7GHz available May 2002 1.8GHz available June 2002
Chipset support	**Intel 845 family**

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Intel® Celeron® for value desktop (and mobile) systems

Code name	**Celeron Northwood**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD SSE2	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions) / Streaming SIMD Extensions 2 (144 new instructions)
L1 cache - bus	256-bit data path / full speed
L1 data cache	8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**128KB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
Frontside bus	**400MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz
Frontside bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software
Cache line size	128 bytes (32 bytes x 4 chunks); burst mode bus of addr-data-data-data
Multiple processors	No SMP support
Technology (micron)	0.13u
Package and connector	**Flip-Chip Pin Grid Array-2 (FC-PGA2) requires 478-pin surface mount Zero Insertion Force (ZIF) socket named mPGA478B socket; used with SDRAM-based chipset (such as 845 chipset)**
Frequency (MHz) and available date	2.0GHz available September 2002 2.1GHz available November 2002 2.2GHz available November 2002 2.2GHz available June 2003 for mobile systems 2.3GHz available March 2003 2.3GHz available June 2003 for mobile systems 2.4GHz available March 2003 2.4GHz available June 2003 for mobile systems 2.5GHz available June 2003 for both desktop and mobile systems (transportable processors) 2.6GHz available June 2003 for both desktop and mobile systems (transportable processors) 2.7GHz available September 2003 for both desktop and mobile systems (transportable processors) 2.8GHz available November 2003 for both desktop and mobile systems (transportable processors)
Chipset support	**Intel 845 and 865 desktop family and others** **Intel 852GM, 852GME, 852PM mobile chipset**

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PC Processors (Mobile Celeron) - Fall 2001

Mobile Intel® Celeron® Processor		
Vendor	Intel®	*Same*
Positioning	Value mobile PC	*Same*
Instruction architecture	IA-32 / P6 microarchitecture / CISC/RISC/micro-ops	*Same*
MMX™ / Streaming SIMD	MMX (57 new instructions) / Streaming SIMD Extensions (70 new instructions)	MMX (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
L1 cache - size	**16KB data; 16KB instruction**	*Same*
L1 cache - write policy	Write-back or thru (data); write-thru (instruction)	*Same*
L1 cache - organization	4-way set associative	*Same*
L1 cache - bus	64-bit / full speed / non-blocking	*Same*
L1 cache - parity	Parity in cache and internal registers	*Same*
L2 cache - size	**128KB / full speed**	**256KB / full speed** (Advanced Transfer Cache)
L2 cache - data path	64-bit data path / ECC	**256-bit data path / quad-wide cache line / ECC**
L2 cache - buffering		Intelligent buffering of read and stores (called Advanced System Buffering with 4 writeback buffers, 6 fill buffers, 8 bus queue entries) / Data Prefetch Logic
L2 cache - organization	8-way set associative / non-blocking	8-way set associative
L2 cache - controller	Integrated / unified (internal die; on die)	Integrated / unified (internal die; on die)
L2 cache - write policy	Write-through or write-back (programmable per line), uncacheable, write-protect	Write-through or write-back (programmable per line), uncacheable, write-protect
L2 cache - type		Non-blocking / pipelined burst synchronous
System bus - parity	ECC on system bus; parity on address bus (frontside)	*Same*
System bus - speed	**133MHz frontside bus**	**100MHz or 133MHz frontside bus**
System bus - features	Nonblocking cache hierarchy	*Same*
Bus architecture	Independent backside and frontside buses operate concurrently / Dual Independent Bus Architecture	*Same*
Execution units	2 integer/MMX units; 1 floating pt unit;1 load unit; 1 store unit	*Same*
Pipeline stages	Decoupled, 14 stage superpipelined	*Same*
Supscal dispatch/execute	5 micro-ops per cycle (3 micro-ops is typical)	*Same*
Superscalar issue	6 micro-ops per cycle (3 micro-ops is typical)	*Same*
Superscalar retire	3 micro-ops per cycle	*Same*
Out-of-order instructions	Yes (called dynamic execution)	*Same*
Branch prediction	Dynamic (based on history) / 512 entry BTB	*Same*
Speculative execution	Yes	*Same*
Math coprocessor	Pipelined math coprocessor	*Same*
Internal processing	32-bits (300 bit internal bus width) / 32-bit word size	*Same*
External data bus	64-bit system bus with ECC	*Same*
External address bus	36-bits (64GB physical address space; 64TB virtual)	*Same*
User registers	8 GPR, 8 FP, 40 more GPR via register renaming	*Same*
Cache line size	32 bytes (8 bytes x 4 chunks)	*Same*
Power management	Quick Start and Deep Sleep	*Same*
Multiple processors	No SMP support	*Same*
Technology (micron)	**0.18u**	**0.13u**
CPU voltage	1.7 volts	1.1 volts for Ultra Low Voltage processors 1.15 volts for Low Voltage processors 1.4 or 1.45 volts for others
Package type	Micro-Flip Chip Ball Grid Array (Micro-FCBGA) Micro-Flip Chip Pin Grid Array (Micro-FCPGA)	Micro-Flip Chip Ball Grid Array (Micro-FCBGA) Micro-Flip Chip Pin Grid Array (Micro-FCPGA)
Frequency (available)	**733MHz** (October 2001) **800A MHz** (October 2001) **866MHz** (October 2001) **933MHz** (October 2001) *The "A" is added to the "800A" in Micro-FCBGA and Micro-FCPGA to distinguish it from the Mobile Intel Celeron Processor 800MHz in Micro-BGA2 and Micro-PGA2 packages*	**650/100MHz Ultra Low Voltage** (January 2002) **650/100MHz Low Voltage** (October 2001) **700MHz/100MHz Ultra Low Voltage** (September 2002) **733MHz/133MHz Low Voltage** (April 2002) **733MHz/133MHz Ultra Low Voltage** (September 2002) **800MHz/133MHz Ultra Low Voltage** (January 2003) **866MHz/133MHz Low Voltage** (January 2003) **1GHz/133MHz** (April 2002) **1.06GHz/133MHz** (January 2002) **1.13GHz/133MHz** (January 2002) **1.2GHz/133MHz** (January 2002) **1.33GHz/133MHz** (June 2002)

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Mobile Intel® Celeron® for value mobile systems

Code name	**Northwood**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
Power mgmt technology	AutoHALT, Stop-Grant, Sleep, Deep Sleep
L1 cache - bus	256-bit data path / full speed
L1 data cache	8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**256KB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
System bus	**400MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz
System bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software
Cache line size	128 bytes (32 bytes x 4 chunks); burst mode bus of addr-data-data-data
Multiple processors	No SMP support
Technology (micron)	0.13u
Voltage	1.3 volts
Package and connector	**Micro Flip-Chip Pin Grid Array (uFCPGA) requires 478-pin surface mount Zero Insertion Force (ZIF) socket**
Frequency (MHz) and available date	1.26GHz available April 2003 1.4GHz available June 2002 1.5GHz available June 2002 1.6GHz available September 2002 1.7GHz available September 2002 1.8GHz available September 2002 2.0GHz available January 2003 2.2GHz available April 2003 2.4GHz available June 2003 2.5GHz available November 2003
Chipset support	**Intel 845MZ with DDR-SDRAM memory** **Intel 845MP with DDR-SDRAM memory** **Intel 852GM, 852GME, 852PM with DDR-SDRAM memory** **Other compatible chipsets**

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Intel® Celeron® M processor for mobile systems

Code name	Banias Celeron or ICP-M
Messaging	Based on an architecture designed specifically for mobile computing, the Intel Celeron M processor delivers a balanced level of mobile processor technology and exceptional value in sleeker, lighter notebook designs
Micro-architecture	IA-32 / micro-op fusion, dedicated stack manager, advanced branch prediction, power-optimized processor system bus
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
Power mgmt technology	Auto Halt, Stop Grant, Deep Sleep, Deeper Sleep
L1 cache - bus	256-bit data path / full speed
L1 data cache	32KB data cache / integrated
L1 instruction cache	32KB instruction cache / integrated
L2 cache - size	**512KB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (internal die; on die)
L3 cache	None
System bus	**400MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz
System bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit
Out-of-order instructions	Yes (out-of-order instruction execution)
Branch prediction	Dynamic (based on history)
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software
Multiple processors	No SMP support
Technology (micron)	0.13u
Package and connector	**Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)**

		Voltage	*Thermal Design Power*	*Announce date*
Frequency (MHz/GHz) and available date	**800MHz Ultra Low Voltage**	**1.004 volts**	**7 watts**	January 2004
	1.2GHz	**1.356 volts**	**24.5 watts**	January 2004
	1.3GHz	**1.356 volts**	**24.5 watts**	January 2004

Chipset support	**Intel 855 chipset family** **Intel 852GM** **Other compatible chipsets**

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PC Processors (Pentium III - Tualatin)

Intel® Pentium® III for desktop and entry-level workstations and servers

Code name	**Tualatin** (pronounced "TWO-ala-tin")
Instruction architecture	IA-32 / CISC/RISC/micro-ops
MMX™ / Streaming SIMD	MMX (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
L1 cache - bus	64-bit / full speed
L1 cache - size/controller	16KB data; 16KB instruction / integrated / non-blocking
L1 cache - write policy	Write-back or thru (data); write-thru (instruction)
L1 cache - organization	4 way set associative (data); 2 way set associative (instruction)
L2 cache - size	**256** or **512KB / full speed** (Advanced Transfer Cache)
L2 cache - data path	**256-bit data path / quad-wide cache line / ECC**
L2 cache - buffering	Intelligent buffering of read and stores (called Advanced System Buffering with 4 writeback buffers, 6 fill buffers, 8 bus queue entries)
L2 cache - organization	8-way set associative
L2 cache - controller	Integrated / unified (internal die; on die)
L2 cache - write policy	Write-through or write-back (programmable per line), uncacheable, write-protect
L2 cache - type	Non-blocking / pipelined burst synchronous
Frontside bus - speed	**133MHz**
Memory addressability	64GB memory addressability
System bus - width	64-bit system bus with ECC
System bus - parity	ECC on system bus; parity on address bus (frontside bus)
Execution units	2 integer/MMX units; 1 floating point unit; 1 load unit; 1 store unit
Supscal dispatch/execute	5 micro-ops per cycle (3 micro-ops is typical); Pipeline stages: decoupled, 14 stage superpipelined
Superscalar issue	6 micro-ops per cycle (3 micro-ops is typical)
Superscalar retire	3 micro-ops per cycle
Out-of-order instructions	Yes (called dynamic execution)
Branch prediction	Dynamic (based on history) / 512 entry BTB / typically predicts 10 to 15 nested branches
Speculative execution	Yes (typically 20 to 30 instructions beyond counter with an average of 5 branches)
Math coprocessor	Pipelined math coprocessor
Processor serial number	None
Serial number	Unique processor serial number
Bus architecture	Independent backside and frontside buses operate concurrently / Dual Independent Bus Architecture (DIB)
Internal processing	32-bits (300 bit internal bus width)
User registers	8 GPR, 8 FP, 8 FPscalar and SIMD, 40 more GPR via register renaming
Cache line size	32 bytes (8 bytes x 4 chunks); burst mode bus of addr-data-data-data
Power management	System Management Mode (SMM)
Multiple processors	**Some support 2-way SMP with appropriate chipset support**
Technology (micron)	**0.13u**
Package type	**Flip-Chip Pin Grid Array-2 (FC-PGA2)**
Connector	**Requires Socket 370 (PGA370)**
Frequency (MHz)	**900 MHz Ultra Low Voltage (DP) 512KB L2 cache for entry-level workstations and servers** (announced Jan 2003) **933 MHz Low Voltage with 512KB L2 cache for blade servers** (announced September 2002) **1.0A GHz 256KB L2 cache for desktop, entry-level workstations and servers** (announced August 2001) **1.0 GHz Low Voltage (DP) 512KB L2 cache for entry-level workstations and servers** (announced January 2003) **1.13A GHz 256KB L2 cache for desktop, entry-level workstations and servers** (announced August 2001) **1.13 GHz-S 512KB L2 cache for servers** (announced June 2001) **1.20 GHz 256KB L2 cache for desktop, entry-level workstations and servers** (announce August 2001) **1.26 GHz-S 512KB L2 cache for servers** (announced August 2001) **1.4 GHz-S 512KB L2 cache for servers and blade servers** (announced January 2002)
Chipset support	**Intel 815x, 820x, 840 and others** **ServerWorks® HE-SL and others**
Server blade support	Pentium III at 933MHz and 1.4GHz supported in "Performance Server Blades"

L2 cache bus also called Backside Bus
Memory or system bus also called Frontside Bus

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PC Processors (Mobile Intel Pentium III-M)

Mobile Intel® Pentium® III Processor-M for mobile systems (and server blade systems)

Code name	**Tualatin** (pronounced "TWO-ala-tin")
Instruction architecture	IA-32 / CISC/RISC/micro-ops
MMX™ / Streaming SIMD	MMX (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
Technology	Enhanced Intel SpeedStep™ technology
L1 cache - bus	64-bit / full speed
L1 cache - size/controller	16KB data; 16KB instruction / integrated / non-blocking
L1 cache - write policy	Write-back or thru (data); write-thru (instruction)
L1 cache - organization	4 way set associative (data); 2 way set associative (instruction)
L2 cache - size	**512KB / full speed** (Advanced Transfer Cache) / integrated / unified (internal die; on die)
L2 cache - data path	**256-bit data path / quad-wide cache line / ECC**
L2 cache - buffering	Intelligent buffering of read and stores (called Advanced System Buffering with 4 writeback buffers, 6 fill buffers, 8 bus queue entries) / Data Prefetch Logic
L2 cache - organization	8-way set associative / non-blocking / pipelined burst synchronous
L2 cache - write policy	Write-through or write-back (programmable per line), uncacheable, write-protect
Frontside bus - speed	**133MHz** (some at 100MHz)
Memory addressability	64GB memory addressability
System bus - width	64-bit system bus with ECC
System bus - parity	ECC on system bus; parity on address bus (frontside bus)
Execution units	2 integer/MMX units; 1 floating point unit; 1 load unit; 1 store unit
Supscal dispatch/execute	5 micro-ops per cycle (3 micro-ops is typical); Pipeline stages: decoupled, 14 stage superpipelined
Superscalar issue/retire	Issues 6 micro-ops per cycle (3 micro-ops is typical) / retires 3 micro-ops per cycle
Out-of-order instructions	Yes (called dynamic execution)
Branch prediction	Dynamic (based on history) / 512 entry BTB / typically predicts 10 to 15 nested branches
Speculative execution	Yes (typically 20 to 30 instructions beyond counter with an average of 5 branches)
Math coprocessor	Pipelined math coprocessor
Serial number	Unique processor serial number
Bus architecture	Independent backside and frontside buses operate concurrently / Dual Independent Bus Architecture (DIB)
Internal processing	32-bits (300 bit internal bus width)
User registers	8 GPR, 8 FP, 8 FPscalar and SIMD, 40 more GPR via register renaming
Cache line size	32 bytes (8 bytes x 4 chunks); burst mode bus of addr-data-data-data
Power management	Quick Start, Deep Sleep, Deeper Sleep
Multiple processors	No SMP support (2-way SMP for 800MHz Low Voltage for server blade systems with ServerWorks® ServerSet III LE)
Technology (micron)	0.13u (130-nanometer)
Package type	Micro-FCPGA (Flip-Chip Pin Grid Array) for socketable boards Micro-FCBGA (Flip-Chip Ball Grid Array) for surface mount boards

L2 cache bus also called Backside Bus
Memory or system bus also called Frontside Bus

		Frontside bus	*Maximum Performance Mode*	*Battery Optimized Mode*	*Announce date*
Frequency (MHz)	**700MHz Ultra Low Voltage***	**100MHz**	**700MHz at 1.1V**	**300MHz at 0.95V**	October 2001/Nov 2001*
	733MHz Low Voltage	**133MHz**	**733MHz at 1.15V**	**466MHz at 1.05V**	October 2001
	750MHz Ultra Low Voltage	**100MHz**	**750MHz at 1.1V**	**350MHz at 0.95V**	January 2002
	750MHz Low Voltage	**100MHz**	**750MHz at 1.15V**	**450MHz at 1.05V**	October 2001
	800A MHz Low Voltage	**100MHz**	**800MHz at 1.15V**	**500MHz at 1.05V**	October 2001
	800MHz Low Voltage**	**133MHz**	**800MHz at 1.15V**	**533MHz at 1.05V**	October 2001/Mar 2002**
	800MHz Ultra Low Voltage*	**100MHz**	**800MHz at 1.15V**	**400MHz at 1.05V**	April 2002*
	800MHz Ultra Low Voltage*	**133MHz**	**800MHz at 1.15V**	**400MHz at 1.05V**	April 2002*
	850MHz Low Voltage	**133MHz**	**850MHz at 1.15V**	**500MHz at 1.05V**	January 2002
	850MHz Ultra Low Voltage	**100MHz**	**850MHz at 1.1V**	**400MHz at 0.95V**	September 2002
	866MHz Low Voltage	**133MHz**	**866MHz at 1.15V**	**533MHz at 1.05V**	January 2002
	866MHz	**133MHz**	**866MHz at 1.40V**	**667MHz at 1.15V**	July 2001
	866MHz Ultra Low Voltage	**133MHz**	**866MHz at 1.1V**	**400MHz at 0.95V**	September 2002
	900MHz Ultra Low Voltage	**100MHz**	**900MHz at 1.1V**	**400MHz at 0.95V**	January 2003
	933MHz Ultra Low Voltage	**133MHz**	**933MHz at 1.1V**	**400MHz at 0.95V**	January 2003
	933MHz Low Voltage	**133MHz**	**933MHz at 1.15V**	**533MHz at 1.05V**	April 2002
	933MHz	**133MHz**	**933MHz at 1.40V**	**733MHz at 1.15V**	July 2001
	1GHz	**133MHz**	**1GHz at 1.40V**	**733MHz at 1.15V**	July 2001
	1GHz Low Voltage	**133MHz**	**1GHz at 1.15V**	**533MHz at 1.05V**	September 2002
	1.06GHz	**133MHz**	**1.06GHz at 1.40V**	**733MHz at 1.15V**	July 2001
	1.13GHz	**133MHz**	**1.13GHz at 1.40V**	**733MHz at 1.15V**	July 2001
	1.2GHz	**133MHz**	**1.2GHz at 1.40V**	**800MHz at 1.15V**	October 2001
	1.26GHz	**133MHz**	**1.2GHz at 1.40V**	**800MHz at 1.15V**	September 2002
	1.33GHz	**133MHz**	**1.2GHz at 1.40V**	**800MHz at 1.15V**	September 2002

Chipset support	**Intel 830MP, 830M, 830MG and others**
Server blade support	*** Supported in server blade systems; Micro-FCBGA only; uses Intel 440GX chipset**
	**** Announced March 2002 for server blade systems; Micro-FCBGA only; supports 2-way SMP in server blade systems with ServerWorks ServerSet III LE chipset**

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Mobile Intel® Pentium® 4 Processor-M for mobile systems

Code name	**Mobile Northwood**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
Hyper-Threading	*Some:* Hyper-Threading (HT) Technology (hardware support for multi-threaded applications)
Power mgmt technology	Enhanced Intel SpeedStep™ technology, Stop Grant, Sleep, Deep Sleep, Deeper Sleep
L1 cache - bus	256-bit data path / full speed
L1 data cache	8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**512KB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die)
L3 cache	None
System bus	**400** or **533MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz
System bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software
Cache line size	128 bytes (32 bytes x 4 chunks); burst mode bus of addr-data-data-data
Multiple processors	No SMP support
Technology (micron)	0.13u
Package and connector	*400MHz:* **Micro Flip-Chip Pin Grid Array (uFCPGA) requires 478-pin surface mount Zero Insertion Force (ZIF) socket** *533MHz:* **Micro Flip-Chip Pin Grid Array (uFCPGA2) requires 478-pin surface mount Zero Insertion Force (ZIF) socket**

		System bus	*Maximum Performance Mode*	*Battery Optimized Mode*	*Hyper-Threading (HT) Technology*	*Announce date*
Frequency (MHz)	**1.4GHz**	**400MHz**	1.4GHz at 1.3 volts	1.2GHz at 1.2v (<2 watts avg power)		April 2002
	1.5GHz	**400MHz**	1.5GHz at 1.3 volts	1.2GHz at 1.2v (<2 watts avg power)		April 2002
	1.6GHz	**400MHz**	1.6GHz at 1.3 volts	1.2GHz at 1.2v (<2 watts avg power)		March 2002
	1.7GHz	**400MHz**	1.7GHz at 1.3 volts	1.2GHz at 1.2v (<2 watts avg power)		March 2002
	1.8GHz	**400MHz**	1.8GHz at 1.3 volts	1.2GHz at 1.2v (<2 watts avg power)		April 2002
	1.9GHz	**400MHz**	1.9GHz at 1.3 volts	1.2GHz at 1.2v (<2 watts avg power)		June 2002
	2.0GHz	**400MHz**	2.0GHz at 1.3 volts	1.2GHz at 1.2v (<2 watts avg power)		June 2002
	2.2GHz	**400MHz**	2.2GHz at 1.3 volts	1.2GHz at 1.2v (<2 watts avg power)		Sept 2002
	2.4GHz	**400MHz**	2.4GHz at 1.3 volts	1.2GHz at 1.2v (<2 watts avg power)		Jan 2003
	2.5GHz	**400MHz**	2.5GHz at 1.3 volts	1.2GHz at 1.2v (<2 watts avg power)		April 2003
	2.6GHz	**400MHz**	2.6GHz at 1.3 volts	1.2GHz at 1.2v (<2 watts avg power)		June 2003
	2.40GHz	**533MHz**	2.40GHz at 1.525 v	1.6GHz at 1.2v (<4.5 watts avg power)		June 2003
	2.66GHz	**533MHz**	2.66GHz at 1.525 v	1.6GHz at 1.2v (<4.5 watts avg power)		June 2003
	2.80GHz	**533MHz**	2.80GHz at 1.525 v	1.6GHz at 1.2v (<4.5 watts avg power)		June 2003
	3.06GHz	**533MHz**	3.06GHz at 1.525 v	1.6GHz at 1.2v (<4.5 watts avg power)		June 2003
	2.66GHz	**533MHz**	2.66GHz at 1.525v	1.6GHz at 1.2v (<3.0 watts avg power)	with Hyper-Threading	Sept 2003
	2.80GHz	**533MHz**	2.80GHz at 1.525v	1.6GHz at 1.2v (<3.0 watts avg power)	with Hyper-Threading	Sept 2003
	3.06GHz	**533MHz**	3.06GHz at 1.55v	1.6GHz at 1.2v (<3.0 watts avg power)	with Hyper-Threading	Sept 2003
	3.2GHz	**533MHz**	3.2GHz at 1.55 volts	1.6GHz at 1.2v (<3.0 watts avg power)	with Hyper-Threading	Sept 2003

Chipset support	**Intel 845MZ with DDR-SDRAM memory** **Intel 845MP with DDR-SDRAM memory** **Intel 852GM, 852GME, 852PM with DDR-SDRAM memory**

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Intel® Pentium® M processor for mobile systems

Code name	**Banias**
Branding	Part of the Intel Centrino™ mobile technology when included with an Intel 855 family chipset and Intel PRO/Wireless Network Connection wireless chip
Micro-architecture	IA-32 / micro-op fusion, dedicated stack manager, advanced branch prediction, power-optimized processor system bus
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
Power mgmt technology	Enhanced Intel SpeedStep™ technology, Auto Halt, Stop Grant, Deep Sleep, Deeper Sleep
L1 cache - bus	256-bit data path / full speed
L1 data cache	32KB data cache / integrated
L1 instruction cache	32KB instruction cache / integrated
L2 cache - size	**1MB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / 64 byte cache line size / 8-way set associative / integrated / unified (internal die; on die)
L3 cache	None
System bus	**400MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz
System bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit
Out-of-order instructions	Yes (out-of-order instruction execution)
Branch prediction	Dynamic (based on history)
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit
Compatibility	Compatible with IA-32 software
Multiple processors	No SMP support
Technology (micron)	0.13u
Package and connector	**Micro Flip-Chip Pin Grid Array (Micro-FCPGA) requires 479-pin surface mount Zero Insertion Force (ZIF) socket (mPGA479M socket) or Micro Flip-Chip Ball Grid Array (Micro-FCBGA) for surface mount (479-ball)**

Frequency (MHz/GHz) and available date		*Highest Frequency Mode*	*Lowest Frequency Mode*	*Announce date*
	900MHz Ultra Low Voltage	**900MHz at 1.0 volts**	**600MHz at 0.85 volts**	March 2003
	1.0GHz Ultra Low Voltage	**1.0GHz at 1.0 volts**	**600MHz at 0.85 volts**	June 2003
	1.1GHz Low Voltage	**1.1GHz at 1.18 volts**	**600MHz at 0.96 volts**	March 2003
	1.2GHz Low Voltage	**1.2GHz at 1.18 volts**	**600MHz at 0.96 volts**	June 2003
	1.3GHz	**1.3GHz at 1.5 volts**	**600MHz at 0.96 volts**	March 2003
	1.4GHz	**1.4GHz at 1.5 volts**	**600MHz at 0.96 volts**	March 2003
	1.5GHz	**1.5GHz at 1.5 volts**	**600MHz at 0.96 volts**	March 2003
	1.6GHz	**1.6GHz at 1.5 volts**	**600MHz at 0.96 volts**	March 2003
	1.7GHz	**1.7GHz at 1.5 volts**	**600MHz at 0.96 volts**	June 2003

Chipset support	**Intel 855 chipset family with DDR-SDRAM memory** **Other compatible chipsets**

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Intel® Pentium® 4 for high performance desktop systems

	1.3GHz, 1.4GHz, 1.5GHz, 1.6GHz, 1.7GHz, 1.8GHz, 1.9GHz, 2.0GHz
Code name	**Willamette**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD SSE2	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions) Streaming SIMD Extensions 2 (144 new instructions)
L1 cache - bus	256-bit data path / full speed
L1 data cache	8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**256KB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
Front Side Bus	**400MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200MHz
Front Side Bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software
Cache line size	128 bytes (32 bytes x 4 chunks); burst mode bus of addr-data-data-data
Multiple processors	No SMP support
Technology (micron)	0.18u
Transistors	~42 million with die size of 217 square millimeters
Package and connector	1. **Pin Grid Array (PGA) requires 423-pin Zero Insertion Force (ZIF) socket named Intel Socket 423 (PGA423); used with RDRAM-based 850 chipset** 2. **Flip-Chip Pin Grid Array-2 (FC-PGA2) requires 478-pin surface mount Zero Insertion Force (ZIF) socket named mPGA478B socket; used with SDRAM-based chipset (such as 845 chipset)**
Frequency (MHz) and available date	1.3GHz: 423-pin available January 2001 1.4GHz: 423-pin available November 2000 1.5GHz: 423-pin available November 2000, 478-pin available August 2001 1.6GHz: 423-pin available November 2000, 478-pin available August 2001 1.7GHz: 423-pin available November 2000, 478-pin available August 2001 1.8GHz: 423-pin available November 2000, 478-pin available August 2001 1.9GHz: 423-pin available November 2000, 478-pin available August 2001 2.0GHz: 423-pin available November 2000, 478-pin available August 2001
Chipset support	**Intel 850 with dual channel RDRAM memory** **Intel 845 with SDRAM memory**

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PC Processors (Pentium 4 - Northwood)

Intel® Pentium® 4 for high performance desktop systems

Code name	**Northwood**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD SSE2	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions) Streaming SIMD Extensions 2 (144 new instructions)
Hyper-Threading	*3.06GHz with 533MHz and all 800MHz system bus processors:* Hyper-Threading (HT) Technology (hardware support for multi-threaded applications)
L1 cache - bus	256-bit data path / full speed
L1 data cache	8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**512KB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
L3 cache	None
System bus	**400** or **533** or **800MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200, 266, or 400MHz
Frontside bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software
Cache line size	128 bytes (32 bytes x 4 chunks); burst mode bus of addr-data-data-data
Multiple processors	No SMP support
Technology (micron)	0.13u
Transistors	~55 million
Package and connector	**Flip-Chip Pin Grid Array-2 (FC-PGA2) requires 478-pin surface mount Zero Insertion Force (ZIF) socket named mPGA478B socket**
Frequency and available date	1.6GHz sub-45W TDP (limited to under 45 watts thermal design point; for small form factor desktops); avail Jan 2002 1.8GHz sub-45W TDP (limited to under 45 watts thermal design point; for small form factor desktops); avail Jan 2002 2.0GHz sub-45W TDP (limited to under 45 watts thermal design point; for small form factor desktops); avail Jan 2002 1.8A GHz with 400MHz system bus: available July 2002 2.0A GHz with 400MHz system bus: available January 2002 ("A" signifies the 0.13 micron version, not 0.18 micron) 2.2GHz with 400MHz system bus: available January 2002 2.26GHz with 533MHz system bus: available May 2002 2.4GHz with 400MHz system bus: available April 2002 2.4B GHz with 533MHz system bus: available May 2002 2.4C GHz with 800MHz system bus: available May 2003 with Hyper-Threading Technology 2.5GHz with 400MHz system bus: available August 2002 2.53GHz with 533MHz system bus: available May 2002 2.6GHz with 400MHz system bus: available August 2002 2.6C GHz with 800MHz system bus: available May 2003 with Hyper-Threading Technology 2.66GHz with 533MHz system bus: available August 2002 2.8GHz with 533MHz system bus: available August 2002 2.8C GHz with 800MHz system bus: available May 2003 with Hyper-Threading Technology 3.0GHz with 800MHz system bus: available April 2003 with Hyper-Threading Technology 3.0GHz with 400MHz system bus: available April 2003 (used in ThinkPad G40) 3.06GHz with 533MHz system bus: available November 2002 with Hyper-Threading Technology 3.2GHz with 800MHz system bus: available June 2003 with Hyper-Threading Technology 3.4GHz with 800MHz system bus: available February 2004 with Hyper-Threading Technology
Chipset support	Intel 850 or 850E with dual channel RDRAM memory Intel 845 with SDRAM or DDR-SDRAM memory Intel 865 family with single or dual channel DDR-SDRAM memory (400, 533, or 800 MHz system bus) Intel 875P with single or dual channel DDR-SDRAM memory (800 MHz system bus)

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PC Processors (Pentium 4 - Prescott)

Intel® Pentium® 4 for desktop systems

Code name	**Prescott**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
SSE3	Streaming SIMD Extensions 3 (13 new instructions)
Hyper-Threading	*800MHz system bus processors:* Hyper-Threading (HT) Technology (hardware support for multi-threaded applications)
L1 cache - bus	256-bit data path / full speed
L1 data cache	16KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**1MB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
L3 cache	None
System bus	**533** or **800MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200, 266, or 400MHz
System bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software
Cache line size	128 bytes (32 bytes x 4 chunks); burst mode bus of addr-data-data-data
Multiple processors	No SMP support
Other features	Thermal monitoring, built-in self test, IEEE 1149.1 standard test access port and boundary scan
Technology	90nm (nanometer) or 0.09u (micron)
Package and connector	**Flip-Chip Pin Grid Array (FC-mPGA4) requires 478-pin surface mount Zero Insertion Force (ZIF) socket named mPGA478B socket**

Frequency and available date		
	2.80A GHz with 533MHz system bus	available February 2004
	2.80E GHz with 800MHz system bus with Hyper-Threading Technology	available February 2004
	3.00E GHz with 800MHz system bus with Hyper-Threading Technology	available February 2004
	3.20E GHz with 800MHz system bus with Hyper-Threading Technology	available February 2004
	3.40E GHz with 800MHz system bus with Hyper-Threading Technology	available February 2004

Chipset support	Intel 865 family with single or dual channel DDR-SDRAM memory Intel 875P with single or dual channel DDR-SDRAM memory

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PC Processors (Pentium 4 Extreme Edition)

Intel® Pentium® 4 Extreme Edition for high-end gamers and power users

Code name	None
Formal name	**Intel Pentium 4 Processor with HT Technology Extreme Edition**
Micro-architecture	IA-32 / NetBurst™ (CISC/RISC/micro-ops) / 20 stage pipeline (Hyper-pipelined technology)
MMX™ / Streaming SIMD	MMX™ (57 new instructions) / Streaming SIMD Extensions (70 new instructions)
SSE2	Streaming SIMD Extensions 2 (144 new instructions)
Hyper-Threading	Hyper-Threading (HT) Technology (hardware support for multi-threaded applications)
L1 cache - bus	256-bit data path / full speed
L1 data cache	8KB data cache / 4-way set associative / write-through / 64 byte cache line / integrated
L1 instruction cache	Size not published / holds 12,000 micro-ops / 8-way set associative / integrated / called Execution Trace Cache; caches decoded x86 instructions (micro-ops)
L2 cache - size	**512KB** / full speed (Advanced Transfer Cache)
L2 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 128 byte cache line size (usually divided into two 64 byte sectors) / 8-way set associative / integrated / unified (internal die; on die) / ECC
L3 cache	**2MB** / full speed
L3 cache - data path	256-bit data path (32 bytes) / transfers on each bus clock / 64 byte cache line size / 8-way set associative / write-back / parity / integrated / unified (internal die; on die)
System bus	**800MHz** (transfers data four times per clock) / address bus transfers at two times per clock / 64 byte cache line size
Memory addressability	64GB memory addressability / 36-bit addressing / address bus is double clocked at 200, 266, or 400MHz
Frontside bus - width	64-bit data path
Execution units	2 integer units; 1 floating point units; 1 load unit; 1 store unit Two integer units (or Arithmetic Logic Units) run at two times core frequency (Rapid Execution Engine)
Out-of-order instructions	Yes
Branch prediction	Dynamic (based on history) / 4KB Branch Target Buffer
Speculative execution	Yes (Advanced Dynamic Execution)
Math coprocessor	Pipelined floating point unit / handles 128-bit floating point registers
Compatibility	Compatible with IA-32 software
Cache line size	128 bytes (32 bytes x 4 chunks); burst mode bus of addr-data-data-data
Multiple processors	No SMP support
Technology (micron)	0.13u
Transistors	~108 million
Package and connector	**Flip-Chip Pin Grid Array-2 (FC-PGA2) requires 478-pin surface mount Zero Insertion Force (ZIF) socket named mPGA478B socket**
Frequency and available date	3.2GHz available November 2003 3.4GHz available February 2004
Chipset support	Intel 865 family Intel 875P

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